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GENERATING MULTI-PHASE CLOCK SIGNALS USING HIERARCHICAL DELAYS

Background of the Invention

[0001] This invention relates to circuits and methods for generating multi-phase clock signals. More particularly, this invention relates to circuits and methods for generating multi-phase clock signals using hierarchical delays.

[0002] Circuits that generate multi-phase clock signals typically output a plurality of clock signals phase-shifted in equally-spaced increments relative to a reference clock signal. The output clock signals typically have the same frequency as the reference clock signal. For example, a typical circuit may output four clock signals phase-shifted by 90°, 180°, 270° and 360°, respectively, relative to the reference clock signal. Circuits that generate multi-phase clock signals are often used, for example, in electronic systems having complex timing requirements in which multi-function operations are completed during a single reference clock cycle. Multi-phase clock signals are also used in electronic systems in which an operation extends over more than one reference clock cycle.

[0003] Conventional circuits generate multi-phase clock signals using analog voltage-controlled delay units (VCDs). The phase shifts (i.e., time delays) generated by the VCDs are adjustable and can be controlled by adjusting the supply voltage. VCDs typically require the use of analog charge pumps and loop filters. It is well-known that analog designs are more difficult to mass produce reliably within stated specifications and are less portable to various process technologies than digital designs.

[0004] In view of the foregoing, it would be desirable to provide circuits and methods for generating multi-phase clock signals that rely less on analog components and more on digital components.

Summary of the Invention

[0005] It is an object of this invention to provide circuits and methods for generating multi-phase clock signals that rely less on analog components and more on digital components.

[0006] In accordance with this invention, a circuit comprising a plurality of serially-coupled hierarchical delay units (HDs) outputs clock signals phase-shifted relative to a reference clock signal. Each HD includes either one or two variable delay lines (VDLs) that provide coarse phase adjustment of an associated input clock signal. Each HD also includes one or more phase mixers that provides fine phase adjustment of the input clock signal. Advantageously, circuits of the invention do not include analog VCDs, charge pumps or loop filters.

[0007] The invention also provides methods of generating multi-phase clock signals using HDs.

Brief Description of the Drawings

[0008] The above and other objects and advantages of the invention will be apparent upon consideration of the following detailed description, taken in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout, and in which:

[0009] FIG. 1 is a block diagram of a conventional circuit that uses analog voltage-controlled delay units to generate multi-phase clock signals;

[0010] FIG. 2. is a timing diagram showing the relative phase shifts between the reference and output clock signals of the circuit of FIG. 1 in a "locked" mode of operation;

[0011] FIG. 3 is a block diagram of a circuit that uses hierarchical delay units to generate multi-phase clock signals in accordance with the invention;

[0012] FIGS. 4-6 are block diagrams of various embodiments of the hierarchical delay units of FIG. 3 in accordance with the invention; and

[0013] FIG. 7 is a block diagram of a system that incorporates the invention.

Detailed Description of the Invention

[0014] The invention relates to circuits and methods for generating multi-phase clock signals using hierarchical delay units, eliminating the need for analog VCDs, charge pumps and loop filters.

[0015] FIG. 1 shows a conventional circuit 100 for generating multi-phase clock signals. Circuit 100 includes a plurality of serially-coupled voltage-controlled delay units (VCDs) 102, 104, 106 and 108,

phase detector 110, charge pump 112 and loop filter 114. A reference clock signal is input to VCD 102 (i.e., the first VCD in the serially-coupled chain) at input 116. In "locked" mode of operation, each VCD phase shifts (i.e., time delays) the reference clock signal by about (360/M)°, where M is the total number of VCDs in the serially-coupled chain. VCDs 102, 104, 106 and 108 preferably do not change the frequency of the reference clock signal. In this example, circuit 100 has four VCDs 102, 104, 106 and 108 (i.e., M = 4), and each VCD produces a phase shift of about (360/4)° = 90°. "Locked" mode of circuit 100 is described in greater detail below. VCDs 102, 104, 106 and 108 output clock signals phase-shifted by about 90°, 180°, 270° and 360° relative to the reference clock signal at outputs 118, 120, 122 and 124, respectively.

[0016] FIG. 2 is a timing diagram 200 that shows the relative phase shifts between the reference and output clock signals of circuit 100 in "locked" mode. As shown, VCD 102 outputs clock signal 202 that is 90° out of phase with reference clock signal 204, which is input to circuit 100 at input 116. VCD 104 outputs clock signal 206 that is 180° out of phase with reference clock signal 204. VCD 106 outputs clock signal 208 that is 270° out of phase with reference clock signal 204. VCD 108 outputs clock signal 210 that is 360° (i.e., one full reference clock period) out of phase with reference clock signal 204.

[0017] Returning to FIG. 1, circuit 100 maintains the "locked" condition shown in FIG. 2 as follows: Phase detector 110 receives the reference clock signal at input 126. Phase detector 110 receives the clock

signal output by VCD 108 (i.e., the last VCD in the serially-coupled chain) at input 128. Phase detector 110 compares the phases of these two signals and provides a signal indicating the result of this comparison to charge pump 112. The desired condition is that these signals are 360° out of phase with one another, as shown in FIG. 2. Charge pump 112 causes either an increase or a decrease in the phase shifts produced by VCDs 102, 104, 106 and 108, depending on which is needed to more closely match the desired condition. In particular, charge pump 112 increases the control voltage (V_{ctrl}) supplied to VCDs 102, 104, 106 and 108 when the clock signal output by VCD 108 is phase-shifted greater than 360° relative to the reference clock signal. This causes a decrease in the phase shifts produced by VCDs 102, 104, 106 and 108. Charge pump 112 decreases the control voltage supplied to VCDs 102, 104, 106 and 108 when the clock signal output by VCD 108 is phase-shifted less than 360° relative to the reference clock signal. This causes an increase in the phase shifts produced by VCDs 102, 104, 106 and 108. Loop filter 114 low-pass filters the high frequency components of the signal output by charge pump 112.

[0018] FIG. 3 shows a circuit 300 that can generate multi-phase clock signals in accordance with the invention. Circuit 300 includes a plurality of serially-coupled hierarchical delay units (HDs) 302, 304, 306, 308 and 310, phase detector 312 and logic circuitry 314. A reference clock signal is input to HD 302 (i.e., the first HD in the serially-coupled chain) at input 316. HDs 302, 304, 306, 308 and 310 are preferably substantially identical to one another

in order to provide output clock signals phase-shifted in equally-spaced increments relative to the reference clock signal. Each HD phase shifts (i.e., time delays) the reference clock signal by about (360/M)° in "locked" mode of operation, where M is the total number of HDs in the serially-coupled chain. HDs 302, 304, 306, 308 and 310 preferably do not change the frequency of the reference clock signal. "Locked" mode of circuit 300 is described in greater detail below. HDs 302, 304, 306, 308 and 310 output clock signals phase-shifted relative to the reference clock signal at outputs 318, 320, 322, 324 and 326, respectively.

[0019] Various numbers of HDs can be included in circuit 300 in order to obtain a desired phase distribution of output clock signals. For example, if four HDs are included in circuit 300 (i.e., M = 4), each delay produces a phase shift of about (360/4)° = 90°. This results in four output clock signals phase-shifted relative to the reference clock signal by about 90°, 180°, 270° and 360°. These output clock signals may appear similar to the output clock signals shown in FIG. 2. If eight HDs are included in circuit 300 (i.e., M = 8), each delay produces a phase shift of about (360/8)° = 45°. This results in eight output clock signals phase-shifted relative to the reference clock signal by about 45°, 90°, 135°, 180°, 225°, 270°, 315° and 360°.

[0020] Phase detector 312 and logic circuit 314 maintain the "locked" condition of circuit 300. In particular, phase detector 312 receives the reference clock signal at input 328 and the output signal of HD 310 (i.e., the last HD in the serially-coupled chain) at input 330. Phase detector 312 compares the

phases of these two signals and provides a signal indicating the result of this comparison to logic circuit 314. The desired condition is often that these signals be 360° (i.e., one full reference clock period) out of phase with one another. Other phase relationships are of course possible. Logic circuit 314 causes either an increase or a decrease in the phase-shifts of HDs 302, 304, 306, 308 and 310, depending on which is needed to more closely match the desired condition. Logic circuit 314 may include various numbers and configurations of logic gates, as needed to provide the digital signals required for controlling the HDs of circuit 300. For example, substantially identical HDs that output clock signals phase-shifted in equally-spaced increments relative to the reference clock signal can be controlled by the same digital signals. The design of a suitable logic circuit 314 should be apparent to one of ordinary skill in the art in view of the following description of HDs.

[0021] A hierarchal delay unit (HD) in accordance with the invention provides multiple stages of phase adjustment. In particular, an HD includes a first stage in which either one or two variable delay lines (VDLs) provide "coarse" phase adjustment of an associated input clock signal. The HD also includes one or more stages of phase mixers that provide "fine" phase adjustment relative to the input clock signal.

[0022] FIG. 4 shows an embodiment of an HD having two stages of phase adjustment in accordance with the invention. HD 400 includes VDLs 402 and 404 and phase mixer 406. In the first stage, VDL 402 receives a clock signal at input 408 and a control signal at input 410, and outputs a signal phase-shifted relative

to the input clock signal by a first phase (ϕ_1) at output 412. VDL 404 receives the input clock signal at input 414 and a control signal at input 416, and outputs a signal phase-shifted relative to the input clock signal by a second phase (ϕ_2) at output 418. In the second stage, phase mixer 406 receives the phase-shifted signals from VDLs 402 and 404 and also receives a control signal at input 420. Phase mixer 406 outputs a clock signal having an overall phase shift (ϕ_{OUT}) relative to the input clock signal at output 422. The overall phase shift (ϕ_{OUT}) can be one of N possible phase shifts, evenly spaced apart, between and including ϕ_1 and ϕ_2, where N is characteristic of phase mixer 406 and can be any reasonable number (e.g., 5 or 10). The Nth phase shift of phase mixer 406 that most closely matches the desired phase shift of HD 400 is preferably selected.

[0023] The overall phase shift ϕ_{OUT} of the clock signal output by HD 400 at output 422 can be represented by the following equation:

$$\phi_{OUT} = \phi_1 * (1-K) + \phi_2 * K$$

$$\text{where } K = c/(N-1)$$

$$\text{for } c = 0, 1, \ldots N-1$$

Variable K is a weighting factor of phase mixer 406 that can be one of N possible values and that determines how closely the output phase shift ϕ_{OUT} matches either of the phase shifts ϕ_1 and ϕ_2. This equation is for an ideal phase mixer having zero propagation delay. For K equal to zero, phase mixer 406 outputs a clock signal phase-shifted by ϕ_1. For K equal to (N-1), phase mixer 406 outputs a clock

signal phase-shifted by ϕ_2. For all other values of c, phase mixer 406 outputs a clock signal phase-shifted between ϕ_1 and ϕ_2.

[0024] VDLs 402 and 404 each include delay units that phase shift the clock signal received at respective inputs 408 and 414 by ϕ_1 and ϕ_2, respectively. The delay units of VDLs 402 and 404 may be either analog or digital that can be digitally controlled by logic circuit 314. The number of delay units in a VDL indicates the number of phase shifts (i.e., ϕs) that the VDL can generate. For example, a VDL having five delay units can phase shift its input signal by one of five phases (e.g., $\phi = \theta$, 2θ, 3θ, 4θ or 5θ). Logic circuit 314 sets control signals 410 and 416 of VDLs 410 and 416 such that one of ϕ_1 and ϕ_2 is greater than or equal to the overall phase shift of HD 400, and the other is less than or equal to the overall phase shift. For example, if HD 400 generates an overall phase-shift of 90° relative to the input clock signal, logic circuit 314 sets control signals 410 and 416 such that one of ϕ_1 and ϕ_2 is greater than or equal to 90°, and the other is less than or equal to 90°.

[0025] Control signals 410 and 416 of VDLs 402 and 404 are preferably set such that ϕ_1 and ϕ_2 differ by only one unit phase shift (i.e., $\phi_2 - \phi_1 = \theta$), which is the minimum phase adjustment step size that can be provided by VDLs 402 and 404.

[0026] In another embodiment, HD 400 may include only a single VDL to generate both ϕ_1 and ϕ_2 having a phase difference of one unit phase shift. In particular, the output of a single VDL could be split

into two outputs, one output providing ϕ_1 and the other output feeding into an additional delay unit to provide ϕ_2.

[0027] The minimum phase adjustment step size θ provided by VDLs 402 and 404 can be represented by the following equation:

$$\theta = (tUD/Tref)*360°$$

where tUD is a time delay characteristic of a single delay unit of VDLs 402 and 404 (e.g., 100 or 200 picoseconds (ps)) and Tref is the period of the clock signal input to HD 400. For example, for an input signal having Tref = 10000 ps (i.e., frequency of 100 MHz), and a unit delay having tUD = 100 ps, the minimum phase adjustment step size that can be provided by VDLs 402 and 404 is $\theta = (100/10000)*360° = 3.6°$.

[0028] Phase mixer 406 provides for finer phase adjustment of the output signal relative to the clock input signal. In particular, because phase mixer 406 outputs a clock signal that can have one of N possible phase shifts, evenly spaced apart, between and including ϕ_1 and ϕ_2, it follows that phase mixer 406 reduces the minimum phase adjustment step size that can be provided by HD 400 to θ/N. For example, keeping with the above example where the minimum step size provided by VDLs is 3.6°, a phase mixer 406 with N = 10 would reduce the minimum phase adjustment step size that can be provided by HD 400 to 3.6°/N = 0.36°.

[0029] In accordance with the invention, an HD may include multiple stages of phase mixers to allow for increasingly finer phase adjustment. FIG. 5 shows another embodiment of an HD in accordance with the invention. HD 500 has three stages of phase adjustment

and includes VDLs 502 and 504 and phase mixers 506, 508 and 510. VDLs 502 and 504 form a single stage of "coarse" phase adjustment that may be the same as that of HD 400. Phase mixers 506 and 508 form a first stage of "fine" phase adjustment, and phase mixer 510 forms a second stage of "finer" phase adjustment.

[0030] In particular, each of phase mixers 506 and 508 receives signals from VDLs 502 and 504 phase-shifted by ϕ_1 and ϕ_2. Phase mixers 506 and 508 generate respective output signals 512 and 514 having N_1 possible phase shifts between and including ϕ_1 and ϕ_2. Phase mixer 510 receives signals 512 and 514, and outputs a clock signal at output 516 having an overall phase shift (ϕ_{OUT}) that can be represented by the following equation:

$$\phi_{OUT} = \phi_1 * (1-K) + \phi_2 * K$$
$$\text{where } K = c/(N_1 * N_2 - 1)$$
$$\text{for } c = 0, 1, \ldots N_1 * N_2 - 1$$

and N_2 is the number of possible phase shifts between and including the phase shifts of signals 512 and 514 that can be generated by phase mixer 510. The above equation is for phase mixers 506, 508 and 510 ideally having zero propagation delay. Together, the two stages of phase mixers provide for $N_1 * N_2$ possible phase shifts, evenly spaced apart, between and including ϕ_1 and ϕ_2. Therefore, the two stages of phase mixers reduce the minimum phase adjustment step size from θ (i.e., the minimum step size that can be provided by VDLs 402 and 404) to $\theta/N_1 * N_2$.

[0031] FIG. 6 shows a generalized embodiment of an HD having multiple stages of phase adjustment in accordance with the invention. HD 600 includes a

single stage of "coarse" phase adjustment (formed by VDLs 602 and 604) and Q of stages of "fine" phase adjustment (formed by a plurality of phase mixers). HD 600 outputs a clock signal at output 606 phase-shifted relative to the input clock signal received at input 608. The overall phase shift (ϕ_{OUT}) of the clock signal at output 606 can be represented by the following equation:

$$\phi_{OUT} = \phi_1*(1-K) + \phi_2*K$$
$$\text{where } K = c/(N_1*N_2*...*N_{Q-1}*N_Q-1)$$
$$\text{for } c = 0, 1, ... (N_1*N_2*...*N_{Q-1}*N_Q-1)$$

and N_Q is the number of possible phase shifts that can be produced by the Qth stage of phase mixers. The above equation is for ideal phase mixers having zero propagation delay. Together, the Q stages of "fine" phase adjustment provide $(N_1*N_2*...N_{Q-1}*N_Q)$ possible phase shifts, evenly spaced apart, between and including ϕ_1 and ϕ_2 generated by VDLs 602 and 604, respectively. Thus, Q stages of phase mixers reduce the minimum phase adjustment step size that can be provided by HD 600 from θ (i.e., the minimum step size that can be provided by VDLs 402 and 404) to $\theta/(N_1*N_2*...N_{Q-1}*N_Q)$.

[0032] FIGS. 4-6 have been described herein for clarity primarily in the context of using the control signals from logic circuit 314 to set respective phase mixers such that a signal having an intermediate phase is generated. Note that some or all of the phase mixers can be controlled to output a signal having the same phase as one of the input signals, if such a phase is desired. For example, in some applications, an input signal may need each stage of "fine" phase adjustment formed by various phase mixers in order to

generate an output signal having a desired phase, while in other applications, an input signal may need only some of the stages of phase mixers in order to generate an output signal having a desired phase. Alternatively, if all the stages of phase mixers are not needed to generate a desired output signal, rather than sending the signals through each stage, the output signal can be routed directly to the output from the last stage needed, thus bypassing the remaining stages.

[0033] FIG. 7 shows a system 700 that incorporates the invention. System 700 includes a plurality of DRAM chips 702, a processor 704, a memory controller 706, input devices 708, output devices 710, and optional storage devices 712. DRAM chips 702 include an array of memory cells. One or more DRAM chips 702 also include one or more circuits of the invention to generates multi-phase clock signals using hierarchical delays. The circuits of the invention may, for example, be used to synchronize data output by the DRAMs with an external clock signal (e.g., synchronous DRAM (SDRAM)). Data and control signals are transferred between processor 704 and memory controller 706 via bus 714. Similarly, data and control signals are transferred between memory controller 706 and DRAM chips 702 via bus 716. Input devices 708 can include, for example, a keyboard, a mouse, a touch-pad display screen, or any other appropriate device that allows a user to enter information into system 700. Output devices 710 can include, for example, a video display unit, a printer, or any other appropriate device capable of providing output data to a user. Note that input devices 708 and output devices 710 can alternatively be a single

input/output device. Storage devices 712 can include, for example, one or more disk or tape drives.

[0034] Thus it is seen that circuits and methods for generating multi-phase clock signals using hierarchical delays are provided. One skilled in the art will appreciate that the invention can be practiced by other than the described embodiments, which are presented for purposes of illustration and not of limitation, and the present invention is limited only by the claims which follow.